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Review Study of Low Power Buffer Amplifier for TFT-LCD

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ABSTRACT: This paper try to help in selection of low power Buffer amplifier for TFT-LCD as per the design constraint like high speed, high resolution, low power dissipation. With the help of research find out the class AB buffer amplifier shown good performance with high slew rate at power supply of 1.144MHz, 1.643mW & 1.84V respectively.

Key words: Thin Film Transistor, LCD, Slew rate, Buffer amplifier.

I. INTRODUCTION

Gradual research evaluation in display system specially TFT-LCD. As we know that the TFT-LCD contain different drivers like row driver, column driver, shit register, Gate driver but the buffer amplifier is most important part of TFT-LCD for the requirement of high speed. Speed constraint also achieved column driver & gate driver but the area is more due to several column drivers are needed to fulfill same requirement. Here the gate driver is performing major roll as he responsible to decide the picture display timing by charging and discharging the pixel capacitor row by row.

Second constraint is low power dissipation, unlike static power dissipation. The static power dissipation arises due to improper discharging as well as parasitic device capacitance. Also when power is dissipated, it leads to increase temperature of the chip by which device performance got affected. Power is more critical design constraint in battery powered application; it reduces the battery life if dissipation happened. One more constraint is that the display output of TFT-LCD buffer amplifiers should be driven by step-wise function, by which the output voltage could be settled with horizontal scanning time as per frame frequency according to row of display matrix. This is very important for the improvement of gray levels in accommodation to output voltage swing offered by rail to rail buffer amplifier.

For achieving high open loop gain is to be possible by using low-valued systematic offset voltage with two stage amplifier. For frequency compensation miller capacitance is used which directly control sensible silicon area compensation at high capacitive impedance output node.

II. RELATED WORK

Saeed Sadoni *et al* presented that, a novel high-bandwidth and low-power buffer amplifier is presented for the liquid crystal display applications. This buffer amplifier consists of a folded cascade differential amplifier in the input and a class-AB amplifier in the output, which are designed carefully. The proposed buffer amplifier utilizes a high-performance feedback circuit to increase the bandwidth. It also utilizes a comparator circuit to avoid wasting power. The designed circuit has been simulated in 180nm technology using HSPICE 2008.3. The simulation results show that the bandwidth, power consumption and power supply of the designed circuit are 1.14MHz, 1.64mW and 1.8V, respectively.

Deepak Mishra *et al,* [2] presented associated article. The article states that, for achieving high speed performance by Buffer Amplifier in TFT-LCD application, then researcher should use zero compensation technique for better performance.

In this article Self biased high-speed low-power rail to rail buffer amplifier for LCD is proposed work under class B operation which is suitable for small and large size LCD panel, the Zero compensation is used to enhance the slew rate and settling time the compensation resistor value should be optimized to get the optimal value of slew rate and phase margin, as with large value of compensation resistor we get adequate phase margin but it will increase settling time and vice versa. A prototype of this buffer is implemented on .35 μm CMOS technology it draws only is 8 μA static current. The buffer draws little static current but has a large driving capability during transition phase, full swing is obtained by RAIL TO RAIL operational amplifier and enlarge driving capability is obtained by the use of two comparators [3]. The buffer is 3 μs of rising settling time and 3.2 μs of falling settling time, the active area occupied by the buffer is approximately 3600 μm². The performance of the proposed buffer is compared with previous buffer it is superior in power consumption, low static current and small settling time.

In 2015 HR Kim, *et al,* [3] present new scheme for Buffer amplifier in the form A novel high-speed column-line driving scheme having output buffer amplifiers embedded with polarity multiplexer switches is proposed for use in large-sized thin-film transistor liquid-crystal displays. The proposed driving scheme does not have explicit output-polarity switches, resulting in lower settling time. Experimental results in a 1.2 μm 13.5 V CMOS process indicated that using the proposed driving scheme the settling times to reach 99% of target voltages for the dot and column inversions were improved by up to 48.6%. This driving scheme can be applied to class AB- or class B-type amplifiers for liquid-crystal display column drivers and output buffers controlled by output switches.

Amrita Shukla *et al,* [4] focused on High speed as well as high resolution of TFT LCD displays. For achieving above mentioned goal This paper propose a verilog implementation of high speed buffer amplifier for reduce the quiescent current consumption a current reuse technique is used in the output stage of the buffer amplifier. The proposed buffer amplifier implemented in a 0.25 μA CMOS technology demonstrate that an average value of 0.1 μA static current. The settling time 0.2% of the final voltage is 2 ns under a 30 KΩ resistance and 30 pF capacitance load. The area of buffer amplifier is 23.123 μm * 78.250 μm. Here Inversion method is used which alternates the positive and negative polarities between the liquid-crystal cell with respect to a common backside electrode. There are three inversion methods, which are frame, line and dot inversions for LCD driving. The dot inversion method is preferred in the high resolution displays. A two-stage amplifier requires compensation for stability. Some buffer amplifiers adopt the output node as a dominant pole to achieve enough stability without a Miller capacitance. However, a charge conservation technique is commonly used in some LCD drivers to reduce the dynamic power Dissipation all column lines are isolated from the buffer amplifiers experience no load for a period of time, these amplifiers require the Miller compensation.

Alfio Dario Grasso *et al,* [5] describes a new compact low-power high-speed output buffer which is suitable for large-size LCD panel application. The proposed buffer amplifier can achieve fast driving capabilities with a limited quiescent current consumption by exploiting a dual-path push-pull operation of the output stage. Moreover, a self-biased solution is adopted to control the DC current of the class-AB output section without additional biasing network. The proposed amplifier achieves fast driving performance and offers a rail-to-rail common-mode input range. Enhanced slewing and settling capabilities are achieved through a novel output stage performing dual-path push-pull operation. No additional biasing network is required to set the quiescent conditions of the class-AB output stage, since the output static current is inherently controlled by the input differential stage itself, without additional power dissipation. Experimental results demonstrate that the suggested buffer can drive a 1000-pF capacitive load with a 5.7V/μs slew-rate and a 0.71 - μs settling time, while drawing 32 - μA overall quiescent current from a 5-V power supply.

Devide Marano *et al,* [6] addresses an improved and compact low-power high-speed buffer amplifier topology for large size liquid crystal display drivers. The proposed buffer achieves fast driving performance, draws a low quiescent current and offers a rail-to-rail common-mode input range. The circuit provides enhanced slewing and settling capabilities by realizing a dual-path push-pull operation of the output stage. No additional bias network is required to fix the quiescent conditions of the class-AB output stage, since the output static current is inherently controlled by the input differential stage itself without auxiliary power dissipation. Simulation results demonstrate that the suggested buffer can drive a 1000-pF column line capacitive load with a 5.8-V/μs slew-rate and a 0.75-μs settling time, while drawing only 3-μA quiescent current from a 3-V power supply.

III. TECHNICAL SUMMARY

For achieving better performance in the form of low power dissipation, high speed, better image quality & slew rate, different design of buffer amplifier being popular in past year, like class B amplifier, Class AB amplifier, two stage amplifier & Rail to Rail buffer amplifier, table 1 shown comparative analysis in different amplifiers.

Table 1

	CMOS Tech.	**Power Dissipation**	**Quiescent current**	**Max. Load capacitance**
Class A	0.6 µm	150 µW	5 µA	30 pF
Class AB	180nm	1.64 mW	8.2 µA	1000 pF
Rail to Rail	0.35 µm	66 µW	8 µA	1000 pF
Two Stage	0.5µm	75 µW	32 µA	70 pF

IV. CONCLUSION

This paper present brief study on working of Buffer amplifier circuit design for TFT-LCD and it gives different techniques for future research scholar to choose better technique as per his/her requirement. But the Class AB amplifier shown better performance with respect to high speed, high voltage swing & low power dissipation.

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